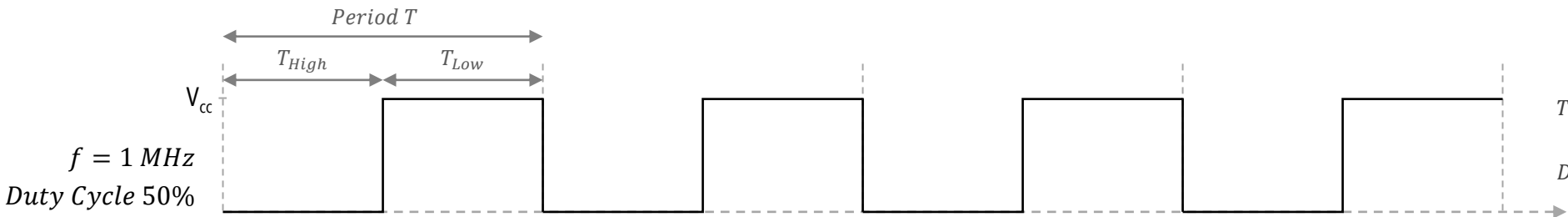
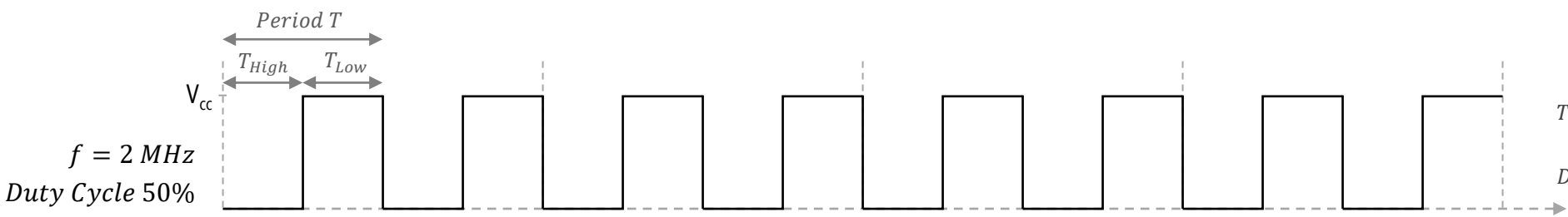


SAME DUTY CYCLE (50%), DIFFERENT FREQUENCIES



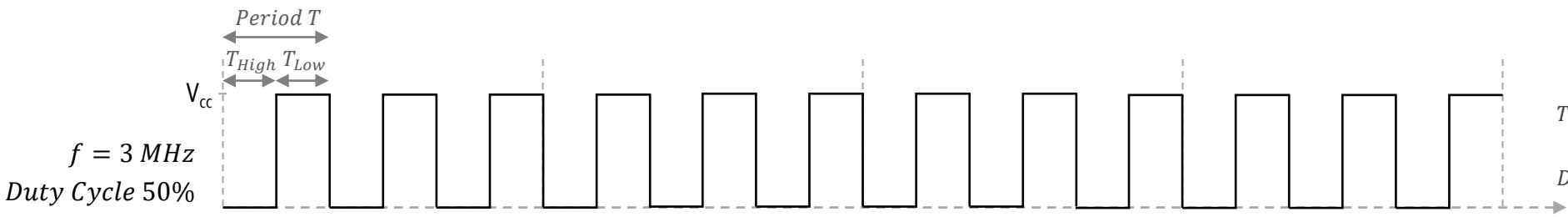
$$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$$

$$\text{Duty Cycle} = \frac{T_{High}}{T} * 100\% \rightarrow \frac{0.5 \mu\text{s}}{1 \mu\text{s}} * 100\% = 50\%$$



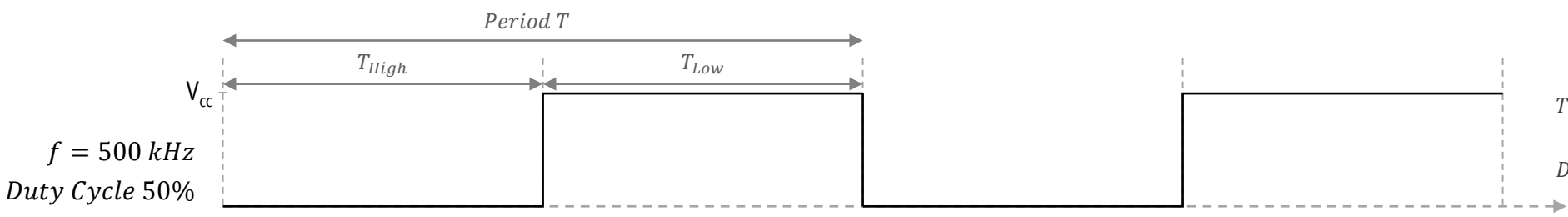
$$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{2 \text{ MHz}} = 0.5 \mu\text{s}$$

$$\text{Duty Cycle} = \frac{T_{High}}{T} * 100\% \rightarrow \frac{0.25 \mu\text{s}}{0.5 \mu\text{s}} * 100\% = 50\%$$



$$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{3 \text{ MHz}} = 0.33 \mu\text{s}$$

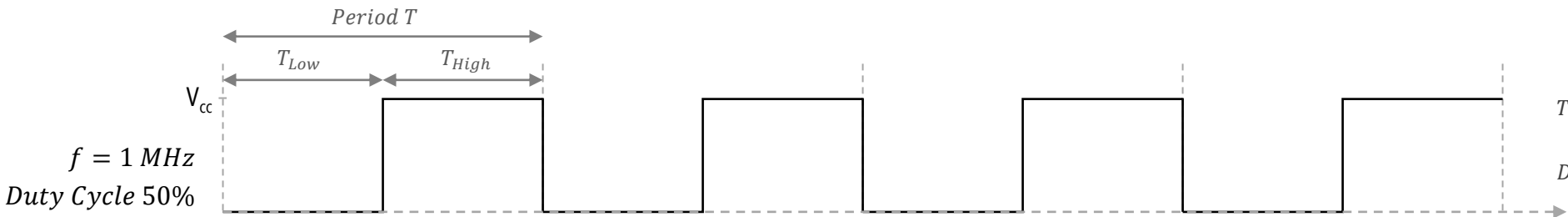
$$\text{Duty Cycle} = \frac{T_{High}}{T} * 100\% \rightarrow \frac{0.16 \mu\text{s}}{0.33 \mu\text{s}} * 100\% = 50\%$$



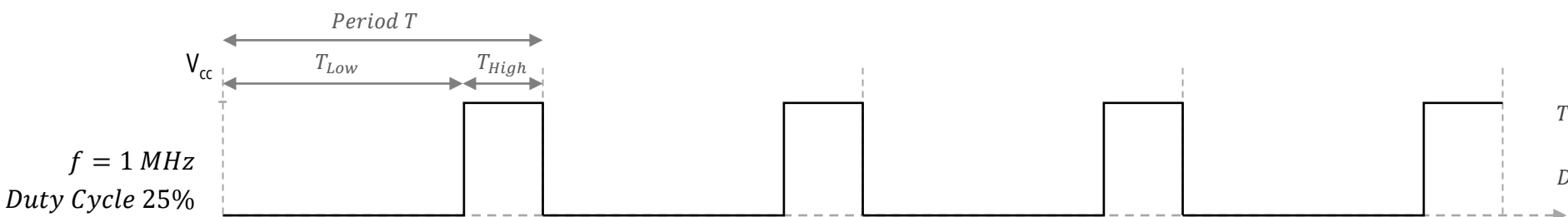
$$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{500 \text{ kHz}} = 2 \mu\text{s}$$

$$\text{Duty Cycle} = \frac{T_{High}}{T} * 100\% \rightarrow \frac{1 \mu\text{s}}{2 \mu\text{s}} * 100\% = 50\%$$

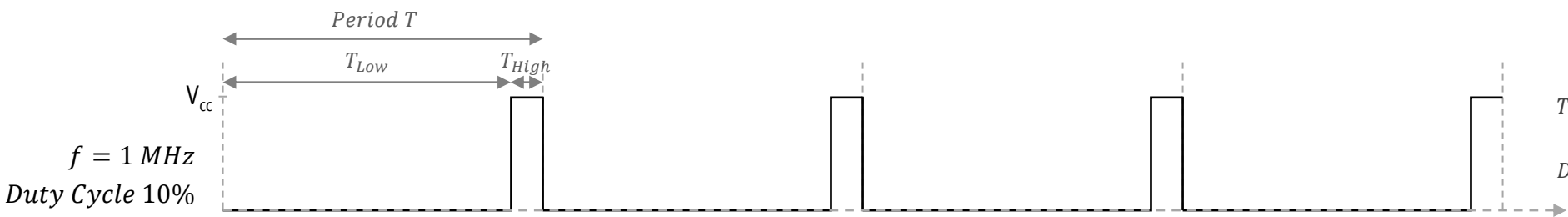
DIFFERENT DUTY CYCLE, SAME FREQUENCY (1MHZ)



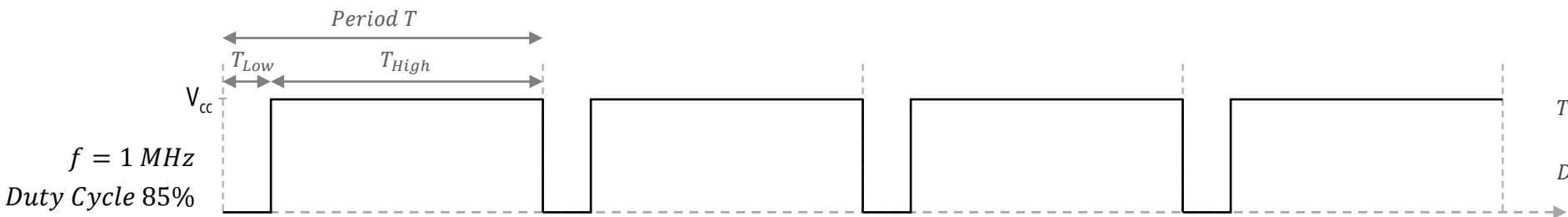
$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$
 $\text{Duty Cycle} = \frac{T_{\text{High}}}{T} * 100\% \rightarrow \frac{0.5 \mu\text{s}}{1 \mu\text{s}} * 100\% = 50\%$



$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$
 $\text{Duty Cycle} = \frac{T_{\text{High}}}{T} * 100\% \rightarrow \frac{0.25 \mu\text{s}}{1 \mu\text{s}} * 100\% = 25\%$



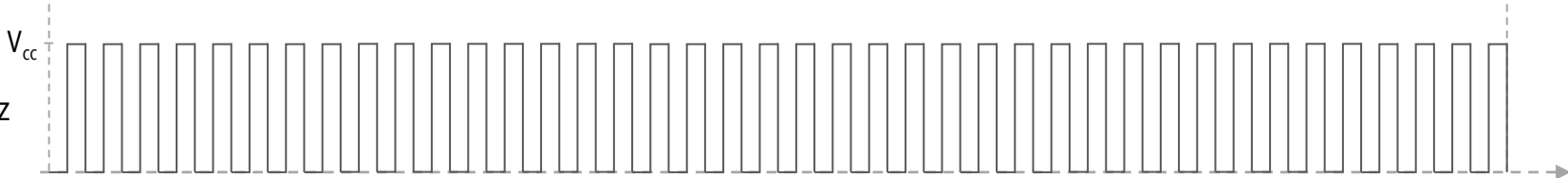
$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$
 $\text{Duty Cycle} = \frac{T_{\text{High}}}{T} * 100\% \rightarrow \frac{0.10 \mu\text{s}}{1 \mu\text{s}} * 100\% = 10\%$



$T = \frac{1}{f} \text{secs} \rightarrow \frac{1}{1 \text{ MHz}} = 1 \mu\text{s}$
 $\text{Duty Cycle} = \frac{T_{\text{High}}}{T} * 100\% \rightarrow \frac{0.85 \mu\text{s}}{1 \mu\text{s}} * 100\% = 85\%$

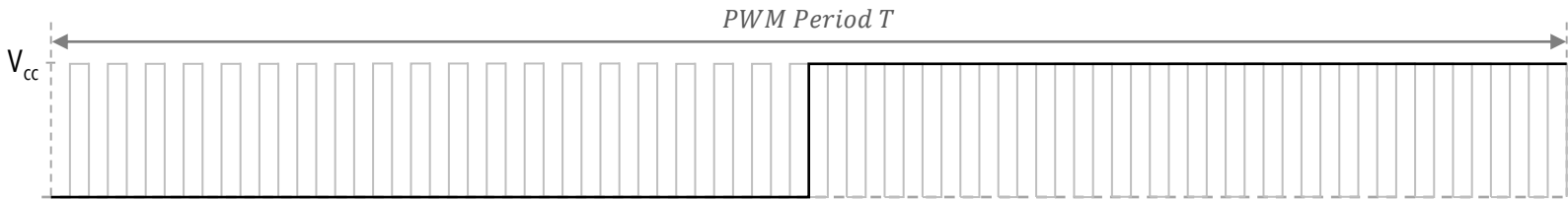
FREQUENCY AND DUTY CYCLE RESOLUTION

Clock frequency = 40 MHz



PWM frequency = 1 MHz

PWM duty cycle = 50%



PWM resolution = 1 bit

2 bits

3 bits

4 bits

5 bits

6 bits

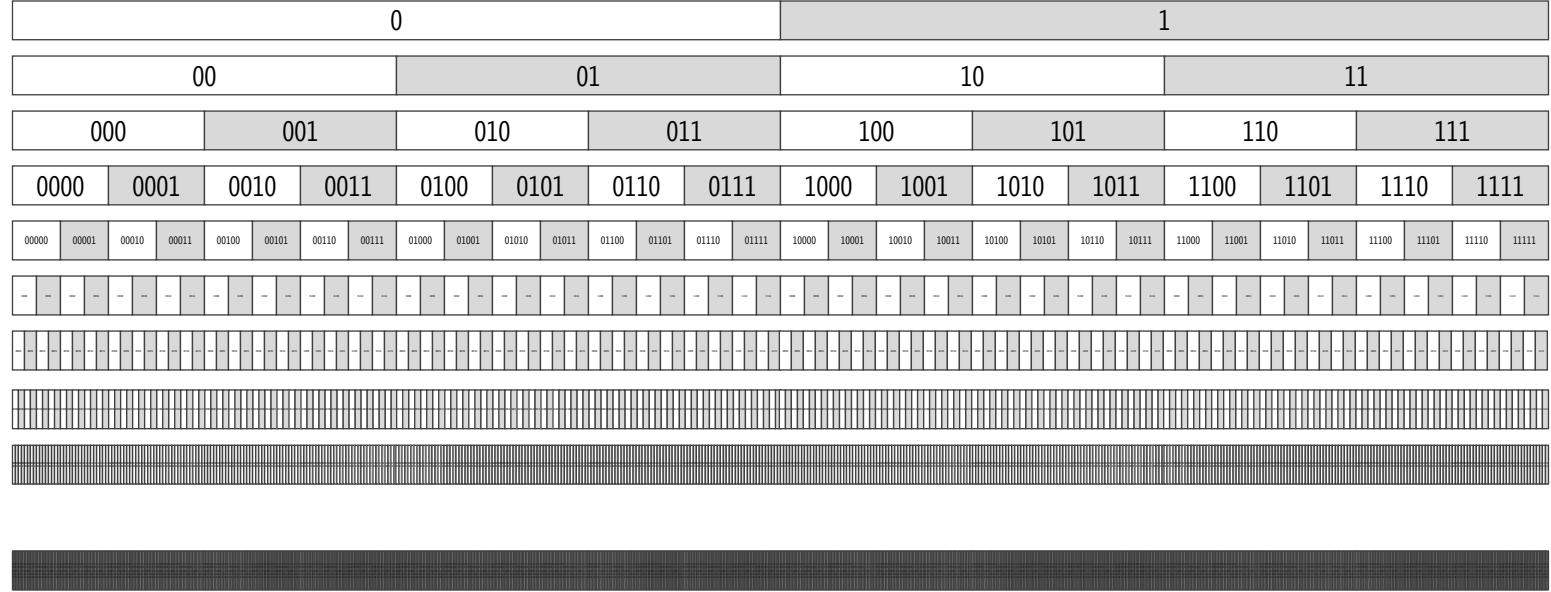
7 bits

8 bits

9 bits

...

16 bits



Bits	Duty Cycle Resolution	Voltage Resolution	Minimum Required Clock* with PWM freq=1MHz
1	Fixed at 50%	Fixed at 1.65V	1 MHz
2	25%	825 mV	4 MHz
3	12.5%	412.5 mV	8 MHz
4	6.25%	206.25 mV	16 MHz
5	3.125%	103.13 mV	32 MHz
6	1.5625%	51.56 mV	64 MHz
7	0.78125%	25.78 mV	128 MHz
8	0.39063%	12.89 mV	256 MHz
9	0.19531%	6.45 mV	512 MHz
...			
16 bits	0.00153%	0.0504 mV	65.536 GHz

*Min clock freq = PWM freq * 2^{resolution}